IN THE SPECIFICATION

Amendments to the Specification:

Please amend paragraphs **[0019]**, **[0049]**, **[0050]** and **[0056]** as the following:

[0019] FIGS. 8A, 8B and 8C show a top view, a side view and an elevational view of an eight-metal-layer unit cell, respectively. FIG. 8D shows the cross-sectional view along with line A-A' in FIG. 8C.

[0049] Accompanied with miniaturization and multi-layer metals in CMOS photolithography process and in multi-layer circuit board manufacturing process, the single-layer unit cells of the upper-layer and lower metal layers shown in FIGS. 1A and 1B can be extended into multi-layer metal designs. FIGS. 8A, 8B and 8C show a top view, a side view and an elevational view of a unit cell having eight metal layers, respectively. FIG. 8D shows the cross-sectional view along with line A-A' in FIG. 8C.

[0050] In this embodiment, lower four metal layers 8001, 8002, 8003 and 8004, and dielectric layers 9001, 9002 and 9003 lain in between, form a thick lower layer of a CCS two-dimensional waveguide structure. Four upper metal layers 8005, 8006, 8007 and 8008, and dielectric layers 9005, 9006 and 9007 lain in between, form an upper layer of the CCS two-dimensional waveguide structure. ~~Each metal layer and adjacent metal layers may be perforated with dielectric openings filled with metal. Due to large amounts of the openings, only conducted metal layers are shown in the diagram.~~ Each dielectric layer sandwiched between two upper metal layers or between two lower metal layers may be perforated with a plurality of openings and filled with metal, i.e., the conducting via 8010 as shown in FIG. 8D. Using such method, attenuation constant of the CCS waveguide metal loss with respect to the CCS two-dimensional waveguide is substantially reduced. Observed from the above, the design of the CCS unit cell formed by the eight metal layers is still similar to the figure of the unit cell shown in FIG. 1. However, there are two major distinctions:

(a) the upper and lower metal layers of the CCS unit cell are replaced by a multi-layer metal layer and dielectric layers having a plurality of openings filled with the metal; and

(b) the dimension or the period P of the unit cell shown in FIGS. 8A, 8B, 8C and 8~~C~~D is far smaller than those shown in FIGS. 1A and 1B because CMOS photolithography processes have higher precisions. In the embodiment shown in FIGS. 8A, 8B, 8C and 8~~C~~D, the period P is set as 28μm.

[0056] Another embodiment of CCS transmission line application in miniaturized integrated circuits shall be illustrated. Referring to FIG. 14 showing a microwave oscillator, two CMOS ~~cross-coupld~~ cross-coupled pairs 362 and 364 are used for producing a negative resistance, and oscillation is generated in conjunction with a CCS transmission line. A CCS transmission line 363 is formed using the square unit cell shown in FIG. 8A along with the multi-layer designs shown in FIGS. 8B, 8C and 8~~C~~D. The CCS transmission line 363 resonates with the CMOS cross-coupled pair 362 and the CMOS cross-coupled pair 364 at an oscillation frequency. The particular frequency is determined by the CCS transmission line and parasitic capacitances of the CMOS cross-coupled pair 362, the cross-coupled pair 364, a buffer amplifier 361 and a buffer amplifier 365, and is largely depended on the CCS transmission line 363 for stability thereof. FIG. 15 shows a preferred embodiment illustrating a CMOS oscillator manufactured from TSMC 0.25μm CMOS RFIC 5-layered metal process. Dimensions of a test chip are 0.5mm × 0.6mm, with actual dimensions of the oscillator being merely 0.26mm × 0.45mm. Two inverted outputs of the oscillator are outputted at a radio frequency (RF) output 366 and an RF output 367, wherein the RF output 366 and the RF output 367 are further outputted via the buffer amplifier 361 and the buffer amplifier 365. Referring to FIG. 15, a 2.5V direct-current (DC) voltage is inputted at a DC supply 368 and a DC supply 369. The DC supply 368 supplies current to a bias network 370, the buffer amplifier 361 and the buffer amplifier 365. The DC supply 369 supplies current to the CMOS cross-coupled pair 362 and the CMOS cross-coupled pair 364. According to the design manual of TSMC 0.25μm CMOS RFIC, the RF output 366 and the RF output 367 are connected with a loading of 50Ω, and simulation results of ADS transient and harmonic balance using Agilent are indicated as in FIGS. 16A and 16B. FIG. 16A shows a spectrum diagram of the RF output 366 after performing Fourier transform with respect to the RF output 366. Output signals thereof oscillate at 4.06GHz, while having an output power at -

22.097dBm and a 2nd harmonic suppression of -29.207dBc. FIG. 16B shows phase noise of the RF output 366 calculated by using ADS harmonic balance, and the simulation results indicate that the phase noise of the oscillator located at 600KHz from a carrier is -95.06dBc/Hz@600KHz.